Amendments to the Specification

Replace paragraph 0042 of the specification with the following paragraph 0042:

[0042] Step **102** involves configuring the circuit in a first test mode by setting both register bits **Q1** and **Q0** to logic 1 which will suppress future updating of BSR latches during the Update-DR state of the TAP, cause future updating of the BSR to occur during the RTI state of the TAP, and de-assert ***forceDisable*** during the Capture-DR ~~sate~~ state. This is achieved by either loading an instruction which includes bits **Q1** and **Q0** or loading an instruction which accesses a separate data register which includes bits **Q1** and **Q0**.